Triangular Multicarrier SPWM Technique for Nine Level Cascaded Inverter

A.Mahendran, K.Muthulakshmi, R.Nagarajan

Abstract-In this paper, novel pulse width modulation technique which uses triangular carrier waveform is proposed for nine-level cascaded inverter. In triangular carrier waveform, different techniques such as phase disposition (PD), inverted phase disposition (IPD), phase opposition disposition (POD) and alternative phase opposition disposition (APOD) are implemented. The fundamental output voltage and harmonics obtained in each method are compared with each other. The proposed switching technique enhances the fundamental component of the output voltage and improves total harmonic distortion. The different PWM methodologies adopting the constant switching frequency multicarrier are simulated for a 1KW, 3f inverter using MATLAB/SIMULINK. The effect of switching frequency on the fundamental output voltage and harmonics are also analyzed.

Index Terms-Sinusoidal Pulse Width Modulation (SPWM), Triangular Multicarrier SPWM (TMC SPWM), Total Harmonic Distortion (THD).

———————————— ◆ ————————————

1 INTRODUCTION

Multilevel inverter is an effective solution for increasing power and reducing harmonics of ac waveform [1]. Multilevel inverters are suitable for high voltage and high power applications due to their ability to synthesize waveforms with better harmonics and important for power electronics applications such as flexible ac transmission systems, renewable energy sources, uninterruptible power supplies, and electrical drives and active power filters. In this paper, constant switching frequency multicarrier [2], [3], pulse width modulation method is used for the multi level inverter. The control objective is to compare the reference sine wave with multicarrier waves for three phase nine level cascaded inverter.

Multilevel voltage source inverter (MVSI) structure is very popular especially in high power DC to AC power conversion applications. It offers several advantages that make it preferable over the conventional voltage source inverter (VSI). These include the capability to handle higher DC link voltage, improved harmonics performance, reduced power device stress [4]. There is a problem in controlling a VSI with variable amplitude and frequency to obtain an output voltage waveform with sinusoidal shape by using simple control techniques and it can be overcome by MVSI.

The general structure of the MVSI is to synthesize a staircase or multilevel output sinusoidal voltage out of several levels of dc voltages and it can therefore be described as a voltage synthesizer. In conventional VSI, the maximum output voltage is determined by the blocking capability of each device. By using a multilevel structure, the stress on each switching device can be reduced in proportional to the higher voltages. Consequently, in some applications, it is possible to avoid expensive and bulky step-up transformer. Another significant advantage of a multilevel output is better and more sinusoidal voltage waveform. As a result, a lower total harmonic distortion (THD) is obtained. In motor applications, high dv/dt in power supply generates high stress on motor windings and requires additional motor insulation
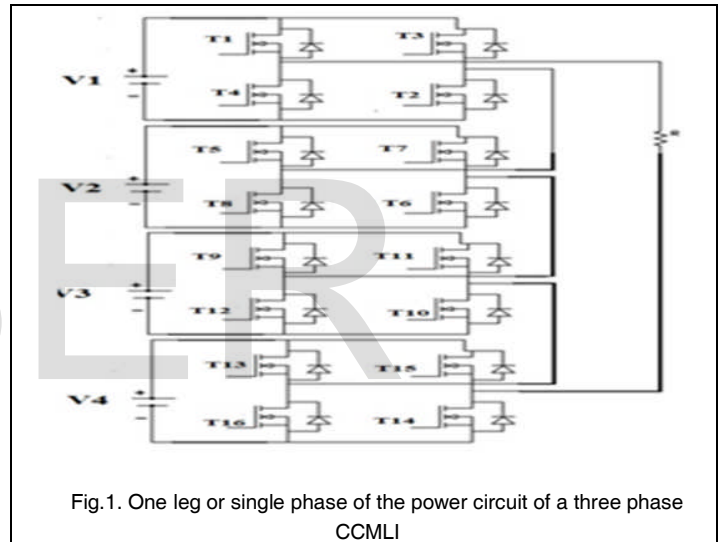

Fig.1. One leg or single phase of the power circuit of a three phase CCMLI

Further, high dv/dt of semiconductor devices increases the electromagnetic interference (EMI), common-mode voltage and possibilities of failure on motor. By increasing the number of levels in the output waveform, the switching dv/dt stress is reduced in the multi level inverter [5], [6].

It is reported that the development of multilevel voltage source inverter topology has began in early 1980's when Nabae at el proposed a three-level neutral point clamped (NPC) Inverter [7]. Later, several multilevel topologies have evolved, such as the Diode Clamped Multilevel Inverter (DCMLI) also known as Neutral Point Clamped (NPC) Inverter, Flying Capacitor Multilevel Inverter (FCMLI) and Cascaded Multilevel Inverter (CCMLI) [8]-[11].

Among them, CCMLI topology is the most attractive, since it requires the least number of components and increases the number of levels in the inverter without requiring high ratings on individual devices and the power rating of the CCMLI is also increased [12]. It also results in simple circuit layout and is modular in structure. Furthermore, CCMLI type of topology is free of

DC voltage balancing problem, which is a common issue facing in the DCMLI and FCMLI topologies. The nine level single phases Cascaded Inverter topology is shown in Fig.1.

2 CASCADED MULTILEVEL INVERTER

The CCMLI consists of a series connection of separate single (full-bridge) or three-phase inverter modules on the ac output terminals [13], [14]. Each dc to ac module requires an isolated dc input. The nine-level CCMLI is having four input DC sources as shown in fig 1. The value of each source is V_{dc}.

Each inverter module can generate three different output voltage levels $+V_{dc}$, 0 and $–V_{dc}$, by connecting the dc source to the output terminals utilizing different switching combinations of the four semiconductor switches in each inverter.

The CCMLI is producing nine level output, they are $4V_{dc}$, $3V_{dc}$, $2V_{dc}$, V_{dc}, 0, $-V_{dc}$, $-2V_{dc}$, $-3V_{dc}$ and $-4V_{dc}$. This topology is suitable for applications where separate dc voltage sources are available, such as photovoltaic (PV) generators, fuel cells and batteries. The phase output voltage is generated by the sum of four output voltage of the full bridge inverter modules. Fig.1 shows the power circuit of one leg of a three phase CCMLI.

The multilevel inverter of Fig.1 utilizes four independent dc sources and consequently will create an output phase voltage with nine levels. In general, if N_s is the number of independent dc sources per phase, then the following relations apply [13]:

$$m = 2N_s + 1 \qquad (1)$$
$$p = 2(m - 1) \qquad (2)$$

Where m is the number of levels and p is the number of switching devices in each phase.
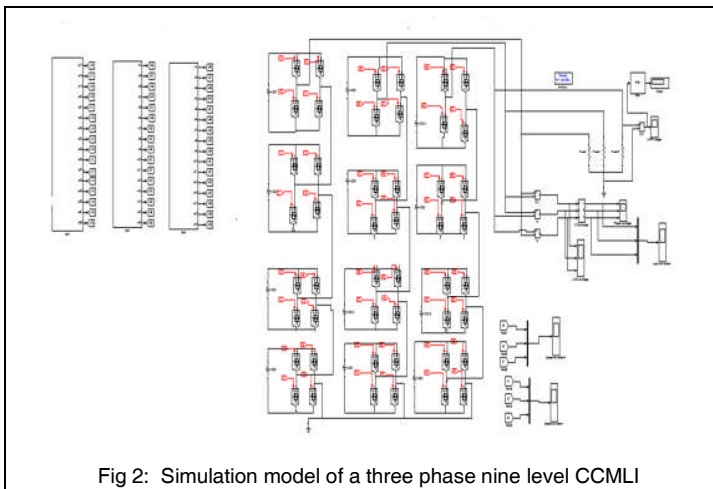

Fig 2: Simulation model of a three phase nine level CCMLI

The most well known SPWM which can be applied to a CCMLI is the Phase-Shifted SPWM. This modulation technique is the same as that of the conventional SPWM technique which is applied to a conventional single-phase full-bridge inverter, the only difference being that it utilizes more than one carrier. The number of carriers to be used per phase is equal to twice the number of dc voltage sources per phase ($2N_s$) [13].

Fig.2 presents the simulation model of a three-phase nine-level CCMLI and is developed using MATLAB/SIMULINK. The simulation results are obtained for the output phase voltage and line voltage of the three-phase nine-level CCMLI with 1KW, 3f resistive loads for various PWM techniques.

3 MODULATION TECHNIQUES

Pulse Width Modulation (PWM) control strategies development tries to reduce the total harmonic distortion (THD) of the output voltage. Increasing the switching frequency of the PWM pattern reduces the lower frequency harmonics by moving the switching frequency carrier harmonic and associated sideband harmonics away from the fundamental frequency component [15]. This increased switching frequency reduces harmonics, which results in a lower THD with high quality output voltage waveforms of desired fundamental RMS value and frequency which are as close as possible to sinusoidal wave shape.

Any deviation in the sinusoidal wave shape will result in harmonic currents in the load and this harmonic current produces the electromagnetic interference (EMI), harmonic losses and torque pulsation in the case of motor drives. Higher switching frequency can be employed for low and medium power inverters, whereas, for high power and medium voltage applications the switching frequency should be low. Harmonic reduction can then be strictly related to the performance of an inverter with any switching strategy. The three phase multi level inverter requires three modulating signals or reference signals which are three sine-waves with 120 degree phase shift.

In this paper, triangular multicarrier sinusoidal PWM (TMC SPWM) technique is developed. Each carrier is to be compared with the corresponding modulating sine wave. The reference or modulation waveform has peak-to-peak amplitude A_m and frequency f_m and it is centered in the middle of the carrier set.

The general principle of a carrier based PWM technique is the comparison of a sinusoidal waveform with a carrier waveform, this typically being a triangular carrier waveform. The reference is continuously compared with the carrier signal. If the reference is greater than the carrier signal, then the active device corresponding to that carrier is switched on, and if the reference is less than the carrier signal, then the active device corresponding to that carrier is switched off [16].

The carrier frequency defines the switching frequency of the converter and the high order harmonic components of the output voltage spectrum and the sidebands occur around the carrier frequency and its multiples. In multilevel inverters, the amplitude modulation index, M_a and the frequency ratio, M_f are defined as [17],

$$M_a = A_m / (m - 1)A_c \qquad (3)$$

$$M_f = f_c / f_m \qquad (4)$$

Where A_m and A_c are amplitude of modulating and carrier signal respectively. f_m and f_c are frequency of modulating and carrier signal respectively. In this paper, modulation index used is unity. For multilevel applications, carrier based PWM techniques with multiple carriers are used. The Multicarrier Modulation (MCM) techniques, can be divided in to the following categories [18] such as,

- Phase disposition (PD) where all the carriers are in phase.
- Inverted phase disposition (IPD) where all the carriers are in phase and is inverted.
- Phase opposition disposition (POD) where the carriers above the zero reference are in phase but shifted by 180 degrees from those carriers below the zero reference.
- Alternative phase opposition disposition (APOD) where each carrier band is shifted by 180 degrees from the adjacent carrier bands [19].

The above modulation strategies are implemented in triangular multi carrier waveform. The line voltage waveform and harmonic spectrum of the line voltage are shown for different modulation techniques by doing simulation using MATLAB/SIMULINK for a nine level CCMLI. The results obtained are compared.

3.1 Triangular Multicarrier Sinusoidal PWM (TMC SPWM)

The performance of the multilevel inverter is based on the multi-carrier modulation technique used. Two-level to multilevel inverters are made using several triangular carrier signals and one reference signal per phase. Carrara [3] developed multilevel sub harmonic PWM (SH-PWM) is as follows,

For m-level inverter, m-1 carriers [15] with the same frequency f_c and same peak to peak amplitude A_c are disposed such that the bands they occupy are contiguous. They are defined as

$$C_i = A_c \left((-1)^{f(i)} y_c (\omega_c, \varphi) + t - (m/2) \right), \qquad (5)$$
$$i = 1,\ldots\ldots (m-1)$$

Where y_c is a normalized symmetrical triangular carrier defined as,

$$y_c (\omega_c, \varphi) = (-1)^{[\alpha]} \left((\alpha \bmod 2) - 1 \right) + 1/2 \qquad (6)$$

$$\alpha = (\omega_c t + \Phi)/\pi = 2\pi f_c \qquad (7)$$

ϕ represents the phase angle of y_c. y_c is a periodic function with the period $T_c = 2\pi/\omega_c$. It is shown that using symmetrical triangular carrier generates less harmonic distortion at the inverters output [20], [21] and is shown in Fig.3.
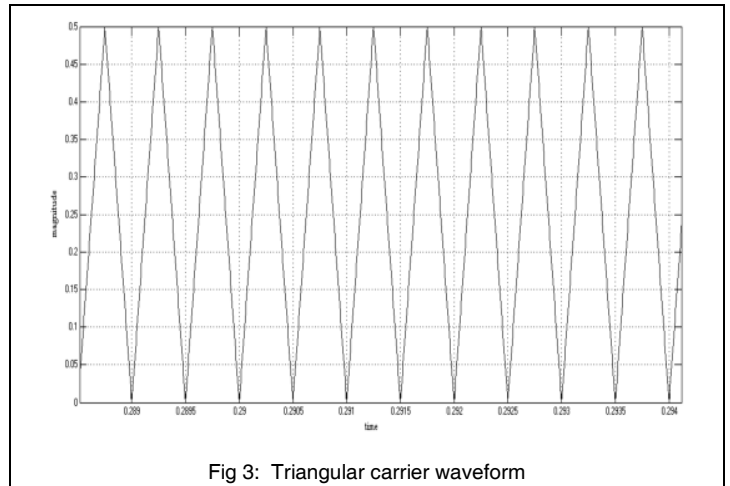

Fig 3: Triangular carrier waveform

The multicarrier modulation techniques (PD, IPD, POD, and APOD) are implemented using triangular multicarrier signals and are shown in Fig. 4(a), 4(b), 4(c) and 4(d) respectively.
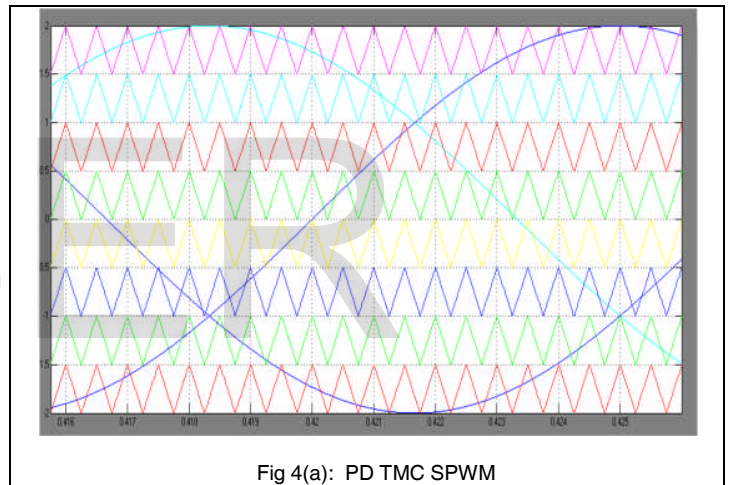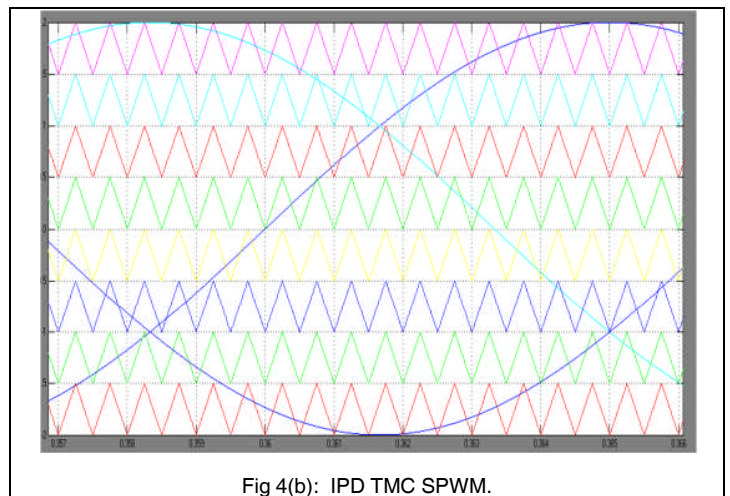

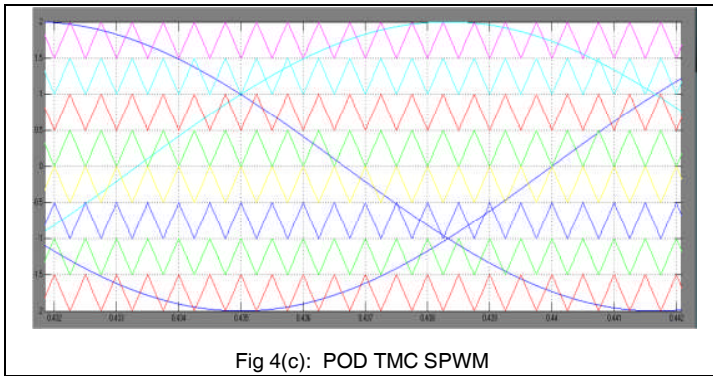Fig 4(a): PD TMC SPWM

Fig 4(b): IPD TMC SPWM.

Fig 4(c): POD TMC SPWM

4.1 Triangular Multi Carrier Modulation Techniques (TMC SPWM)

Fig 5(a): Line Voltage forTriangular Multi Carrier Phase Disposition SPWM
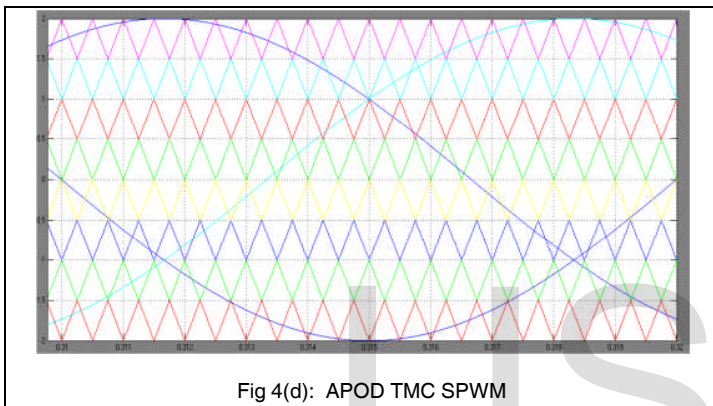

Fig 4(d): APOD TMC SPWM

In TMC SPWM, so far only the PD, POD and APOD techniques are discussed earlier in the literature. In this paper, IPD scheme is also applied to TMC SPWM and it is found that this scheme gives the lowest THD among all other PWM schemes.

Fig 5(b): Percentage Line Voltage THD forTriangular Multi Carrier Phase Disposition SPWM

4. SIMULATION RESULTS

A nine level cascaded multilevel inverter model was implemented in MATLAB/SIMULINK software to demonstrate the feasibility of PWM techniques. Phase disposition, inverted phase disposition, phase opposition disposition and alternative phase opposition disposition techniques are used for the Triangular multicarrier Sinusoidal PWM   techniques.

The line voltage waveform with its harmonic spectrum at fundamental frequency of 50Hz and switching frequency of 2 KHz and 10 KHz is obtained for the proposed CCMLI. For comparison, the total harmonic distortion (THD) was chosen to be evaluated for all the modulation techniques. In order to get THD level of the waveform, a Fast Fourier Transform (FFT) is applied to obtain the spectrum of the output voltage.

Here the %THD is calculated up to a harmonic order which is twice the switching frequency. For 2 KHz switching frequency up to 80th order harmonics is taken in to account for calculating THD and for 10 KHz switching frequency up to 400th order harmonics is taken in to account for calculating THD.

Fig 5(a) and 5(b) show the line voltage and the percentage THD of the line voltage for the triangular multi carrier sinusoidal PWM using phase disposition technique.
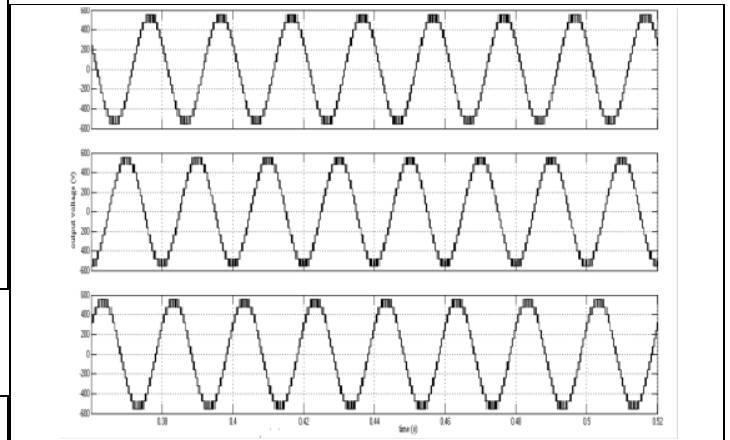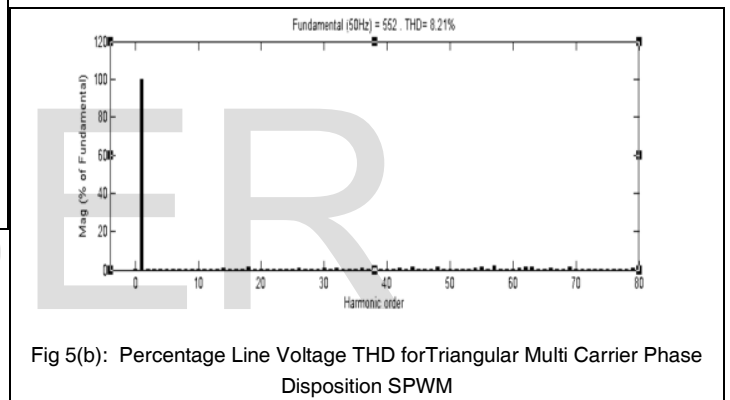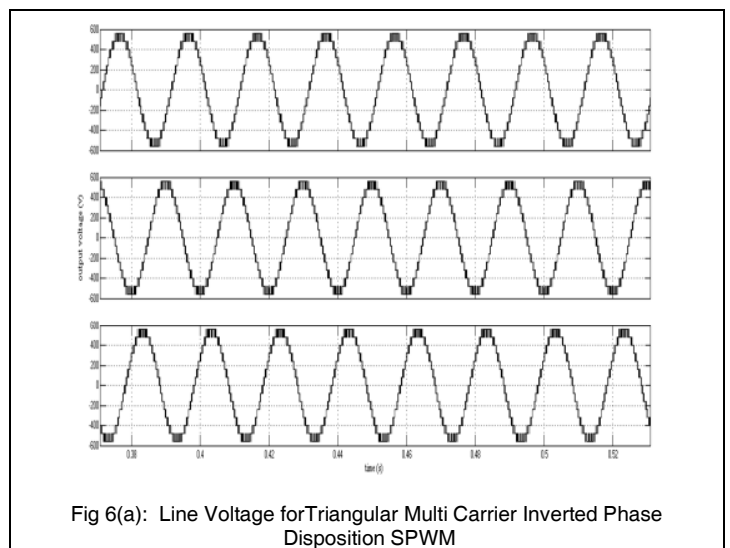

Fig 6(a): Line Voltage forTriangular Multi Carrier Inverted Phase Disposition SPWM

Fig 6(b): Percentage Line Voltage THD for forTriangular Multi Carrier Inverted Phase Disposition SPWM
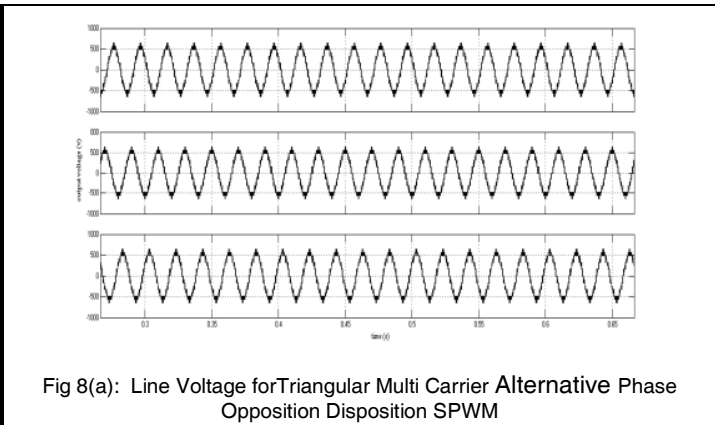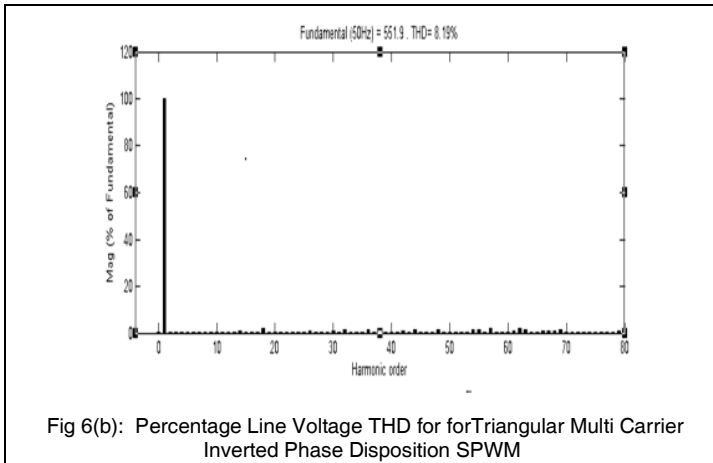
Fig 6(a) and 6(b) show the line voltage and the percentage THD of the line voltage for the triangular multi carrier sinusoidal PWM using inverted phase disposition technique.

Fig 7(a): Line Voltage forTriangular Multi Carrier Phase Opposition Disposition SPWM

Fig 7(b): Percentage Line Voltage THD for Triangular Multi Carrier Phase Opposition Disposition SPWM

Fig 7(a) and 7(b) show the line voltage and the percentage THD of the line voltage for the triangular multi carrier sinusoidal PWM using phase opposition disposition technique.

Fig 8(a): Line Voltage forTriangular Multi Carrier Alternative Phase Opposition Disposition SPWM

Fig 8(b): Percentage Line Voltage THD forTriangular Multi Carrier Alternative Phase Opposition Disposition SPWM
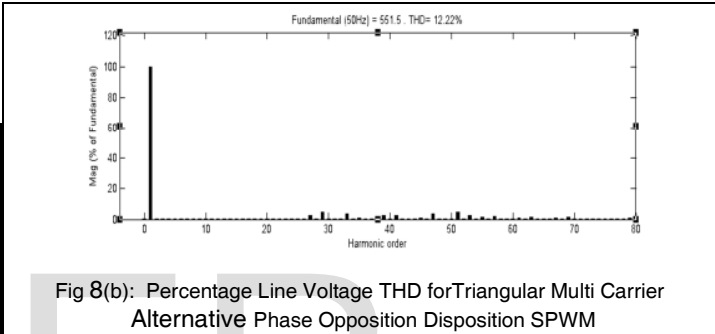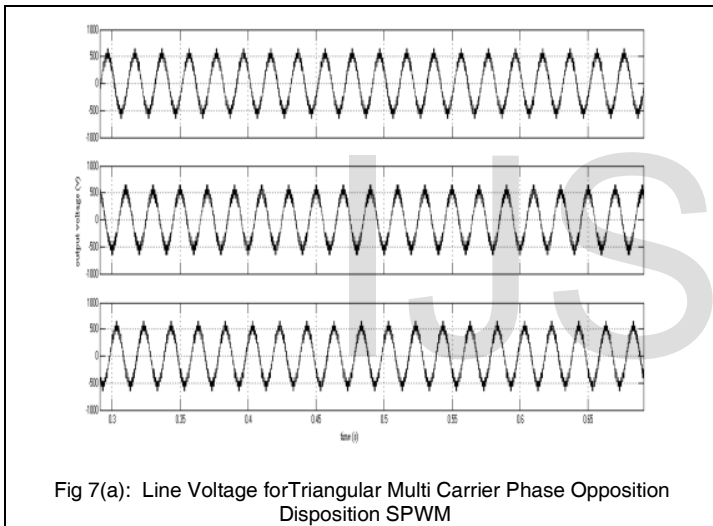
Fig 8(a) and 8(b) show the line voltage and the percentage THD of the line voltage for the triangular multi carrier sinusoidal PWM using alternative phase opposition disposition technique.

Table.1 show the percentage line voltage THD, fundamental phase and line voltage, and dominant harmonic factor are obtained for the different multicarrier PWM techniques with a switching frequency of 2 KHz and 10 KHz respectively.

From the simulation result in the triangular multi carrier SPWM technique PD and IPD PWM schemes, from 3rd order harmonics to 17th order harmonics and higher odd order harmonics (above 17th harmonics) are less than 1%. Few of the even order harmonics from 18th harmonics to 54th harmonics for the above mentioned scheme are less than 2%. The dominant 57th harmonic factor is about 2% for the PD and IPD schemes.

In the POD scheme, from 3rd order harmonics to 19th order harmonics and higher even order harmonics (above 20th harmonics) are less than 1%. Few of the odd order harmonics from 21st harmonics to 69th harmonics are 1% to 2%. The dominant 39th and 41st harmonic factor are 5.37% and 5.59% respectively for the POD scheme.

In the APOD scheme, from 3rd order harmonics to 25th order harmonics and higher even order harmonics (above 26th harmonics) are less than 1%. Few of the higher odd order harmonics above 27th order are present. The dominant 29th and 51st harmonic factor are 4.70% and 4.59% respectively for the APOD scheme.
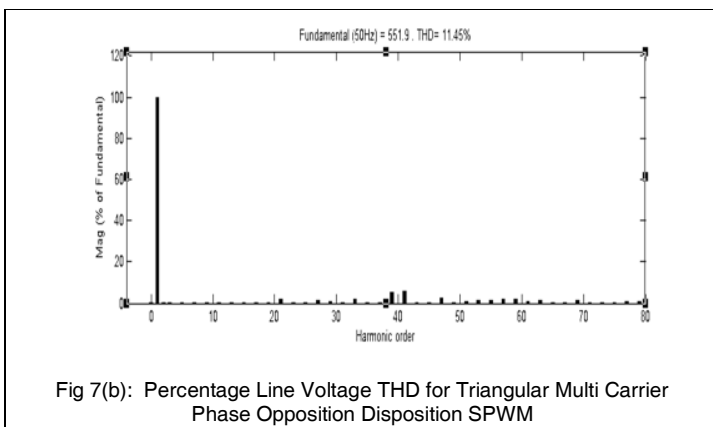
It is observed that, when the switching frequency of the CCMLI is increased, the percentage line voltage THD, the fundamental phase and line voltage are decreased very slightly for the PD and IPD schemes. In the POD and APOD schemes, if the switching frequency is increased, the percentage line voltage THD is increased very slightly and the fundamental phase and line voltage are decreased very slightly. Also the fundamental line voltage is maximum for POD scheme and is minimum for PD and IPD schemes.

TABLE.I
Line voltage %THD, Fundamental voltage per phase, Fundamental line voltage and dominant harmonic factor for triangular multicarrier SPWM

Modulation Technique		Line voltage % THD	Voltage per phase (volts)	Line voltage (volts)	Dominant harmonic factor (%)
FS (2KHz)	PD	8.21	227	391.2	H_{57}=1.83
	IPD	**8.19**	227	391.2	H_{57}=1.84
	POD	11.45	227.1	**392.8**	H_{39}=5.37 H_{41}=5.59
	APOD	12.22	227	**392.7**	H_{29}=4.70 H_{51}=4.59
FS (10KHz)	PD	8.18	226.4	389.9	H_{377}=1.65
	IPD	**8.17**	226.4	389.9	H_{377}=1.66
	POD	12.49	226.7	**392.**	H_{199}=6.01 H_{201}=5.99
	APOD	12.71	226.9	**392.1**	H_{189}=4.85 H_{211}=4.85

5 CONCLUSION

The simulation results for a three phase cascaded nine-level inverter which use triangular carrier wave as novel multicarrier Modulation technique is obtained through MATLAB/SIMULINK. In triangular carrier waveform, different techniques such as phase disposition (PD), inverted phase disposition (IPD), phase opposition disposition (POD) and alternative phase opposition disposition (APOD) are implemented. The output quantities like fundamental phase and line voltage, percentage THD of the line voltage and percentage dominant harmonic factor are being found. When the switching frequency is 2 KHz, phase opposition disposition (POD) scheme gives maximum line voltage and triangular (IPD) scheme gives minimum % THD for line voltage. If the switching frequency is 10 KHz, alternative phase opposition disposition (APOD) scheme gives maximum line voltage and triangular (IPD) scheme gives minimum % THD for line voltage. The proposed methods offer better harmonic performance and selection of proper switching frequency in the pulse width modulation strategies enhances the fundamental output voltage.

REFERENCES

[1]   Mariusz Malinowski, K. Gopakumar, Jose Rodriguezand Marcelo A. Pérez, "A Survey on Cascaded Multilevel Inverters" *IEEE Transactions on Industrial Electronics*, *vol. 57, n. 7,* July 2010, pp 2197 – 2206.

[2]   Jang-Hwan Kim, A carrier-Based PWM Method for Three-Phase Four-Leg Voltage Source Converters", *IEEE transactions on power electronics, vol. 19, n.1,* January 2004.

[3]   G.Carrara, S.Gardella, M.Marchesoni, R.Salutari, G.Sciutto, "A New Multilevel PWM Method: A Theoretical Analysis," *IEEE Trans. Power Electronics, vol. 7, n.3,* July 1992, pp 497-505.

[4]   S.M.Ayob, Z.Salam, "Trapezoidal PWM Scheme for Cascaded Multilevel Inverter" *First International Power and Energy Conference*, November 2006, pp 368-372.

[5]   Rodriguez, Jih-sheng lai, and F.Zheng peng, "Multilevel Inverters; A Survey of Topologies, Controls, and Applications," *IEEE Trans.Ind.Electron, vol.49, n. 4*, pp724-738, Aug.2002.

[6]   Samir koaro, PabloLezana, Mauricio Anguio and Jose Rodriguez, "Multicarrier PWM DC-Link ripple forward compensation for multilevel inverters," IEEE Trans. Power.Electron., *vol.123, n.1,* pp.52-56, Jan 2008.

[7]   Nabae, I. Takahashi, and H. Akagi, (Sep./Oct. 1981) "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl., vol. IA-17, n. 5*, pp. 518–523.

[8]   K.A.Corzine, and Y.L.Familiant, "A New Cascaded Multilevel H-Bridge Drive," *IEEE Trans. Power Electron, vol.17, n.1*, pp. 125-131, Jan 2002.

[9]   R.Teodorescu,F.Blaabjerg, J.K.Pedersen, E.Cengelci, and P.N.Enjeti, "Multilevel Inverter by cascading industrial VSI," *IEEE Trans. Ind. Electron, vol.49, n.4*, pp 832-838, Aug 2002.

[10] J.S.Lai, and F.Z.Peng, "Multilevel converters – A new bread of converters," *IEEE Trans. Ind.Appli., vol.32, n.3*, pp.509-517, May/Jun. 1996.

[11] T.A.Maynard, M.Fadel and N.Aouda, "Modelling of Multilevel converter," *IEEE Trans. Ind.Electron., vol.44*, pp 356-364, Jun.1997.

[12] Panagiotis Panagis, Fotis Stergiopoulos, Pantelis Marabeas and Stefanos Manias, "Comparison of State of the Art Multilevel Inverters" *IEEE Trans*, 2008, pp 4296-4301.

[13] Fang.Z. Peng, John W.Mckeever, and Donald J.Adams, "A Power line conditioner using Cascade Multilevel Inverters for Distribution systems" *IEEE Transactions on Industrial Applications, vol. 34, n.6,* pp 1293-1298, Nov/Dec 1998.

[14] B.P.Mcgrath, D.G.Holmes, "Multicarrier PWM strategies for multilevel inverters," *IEEE Trans. Ind.Electron, vol 49, n.4,* pp 858-867,Aug.2002.

[15] Ms.T.Prathiba, Dr.P.Renuga, "Multi Carrier PWM Based Multi Level Inverter For High Power Applications" *Int. Journal of Computer Applications, vol.1, n. 9,* 2010, pp 67-71.

[16] Lion M.Tolbert and Thomas.G.Habetler, "Novel Multi Level Inverter Carrier Based PWM methods", *IEEE IAS*, 1998, pp 1424-1431.

[17] D.G.Holmes and T.A.Lipo, *Pulse Width Modulation For*

Power Converters (Wiley Inter-science, 2003).

[18] D.G.Holmes and B.P.Mcgrath, "Opportunities for harmonic cancellation with carrier based PWM for two level and multilevel cascaded inverters", in *conf.prec IEEE/IAS Annual meeting*,1999.

[19] C.Govindaraju, Dr.K.Baskaran, "Optimized Hybrid Phase Disposition PWM control method for multilevel inverter" *ACEEE Int. Journal on Electrical and Power Engineering, vol. 1, n. 1*, Jan 2010, pp 36-40.

[20] J.Hamman and F.S.Van Der merwe, "Voltage harmonics generated by voltage fed inverters using PWM natural sampling" *IEEE Trans. Power Electron*, *vol PE-3,n.3*, pp.297-302, Jul.1988.

_____

- *A.Mahendran is currently pursuing master's degree program in Applied Electronics, Kamaraj College of Engineering and Technology in Anna University, Viruthunagari, Tamilnadu, India.   E-mail: maha17am@gmail.com*

- *K.Muthulakshmi is currently working as Associate Professor in Electrical and Electronics Engineering Department, Kamaraj College of Engineering and Technology ,Viruthunagar,Tamilnadu, India*

- *R.Nagarajan is currently working as Associate Professor in Electrical and Electronic Engineering Department, Raja College of Engineering and   Technology in Anna University, Madurai, India. E-mail: knaga71@yahoo.com*